

FIG. 1

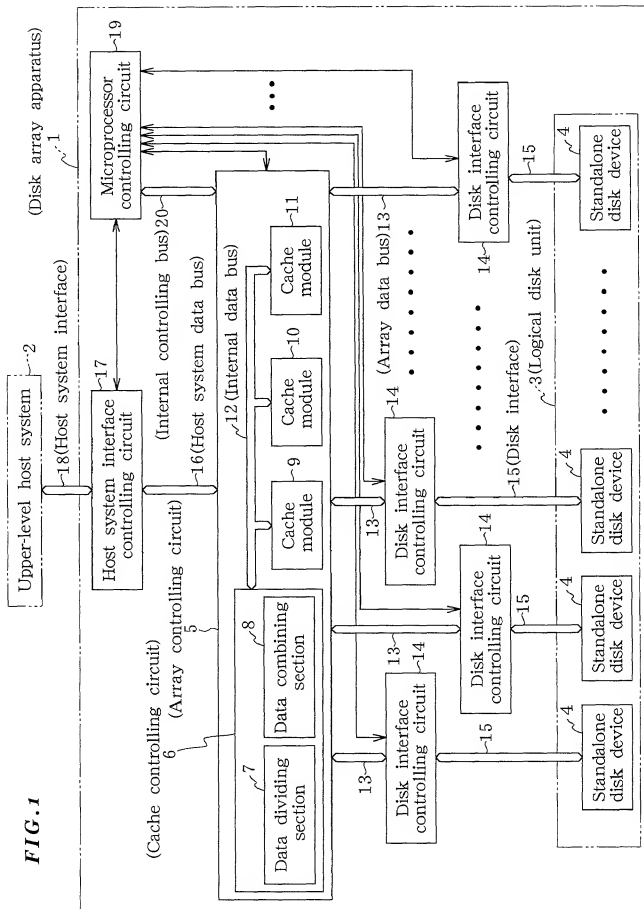
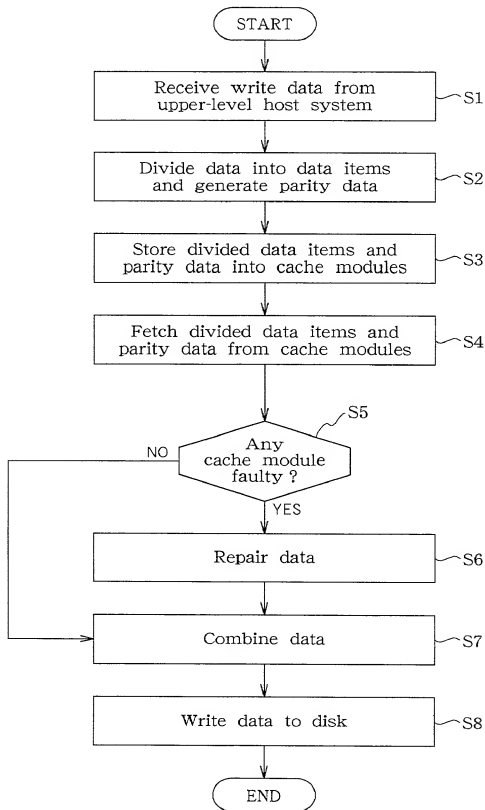


FIG. 2



The diagram illustrates a multi-processor system architecture. At the top, an **Upper-level host system** (102) is connected to a **Host system interface circuit** (101). This interface circuit is connected to a series of **Microprocessor controlling circuit** blocks. Each microprocessor controlling circuit is connected to a corresponding **Host system interface circuit** (101). The host system interface circuit is connected to a **Cache controlling circuit** (112) and a **Cache module** (110). The cache controlling circuit is connected to a **Disk interface circuit**. The disk interface circuit is connected to a **Standalone disk device**. The architecture is shown for multiple microprocessors, with ellipses indicating additional units.

Standalone
disk deviceStandalone
disk deviceStandalone
disk device